AMENDMENTS TO THE CLAIMS:

Please amend the claims by canceling claims 1-22 and adding new claims 24-31.

1.-22. (Cancelled)

23. (Original) A non-volatile memory formed on an integrated circuit substrate, comprising:

an array of memory cells formed in a first region of the substrate,

circuits peripheral to the memory cell array including decoders, drivers and sense amplifiers that are formed in a second region of the substrate that does not overlap the first region, and

a trench formed in the substrate between the first and second regions, the trench being at least 3000 Angstroms in depth and filled with a dielectric material, thereby to isolate the memory cell array and peripheral circuits.

24. (New) A non-volatile memory, comprising:

an array of charge storage elements formed on a semiconductor substrate,

field dielectric material positioned between the charge storage elements in at least one direction across the array, and

electrically conductive control gates extending across tops of the array of charge storage elements in said at least one direction with a layer of dielectric positioned therebetween and protruding downward into slots formed in the field dielectric between adjacent ones of the charge storage elements, the downward portions of the control gates providing electrical shielding between adjacent charge storage elements in said one direction.

25. (New) The memory of claim 24, wherein the individual charge storage elements have different widths across top and bottom portions thereof in said at least one direction, the top portions being wider than the bottom portions, and the control gates protruding downward therebetween a distance at least as great as a thickness of the top portions.

26. (New) The memory of claim 24, wherein the field dielectric is formed over a surface of the semiconductor substrate.

27. (New) The memory of claim 24, wherein the array includes the storage elements arranged in a regular pattern of rows and columns, said at least one direction extending along the columns, and wherein the rows include select gates and source/drain regions in the substrate alternately positioned between adjacent storage elements along the rows.

28. (New) A non-volatile memory, comprising:

a rectangular array of charge storage elements formed on a substrate surface with a first layer of dielectric therebetween, the individual charge storage elements including a first portion positioned against the first dielectric layer with a first width in one direction across the array and a second portion integrally formed with the first portion a distance removed from the first dielectric layer and with a second width in said one direction, said second width being greater than said first width, and

elongated electrically conductive control gates extending in said one direction across surfaces of a plurality of charge storage elements furthest removed from the substrate and with a second layer of dielectric therebetween, the control gates additionally extending between adjacent charge storage elements for a distance at least equal to a thickness of the second portion of the charge storage elements, the extensions of the control gates between adjacent charge storage elements providing electrical shielding in said one direction between at least the second portions thereof.

29. (New) The non-volatile memory of claim 28, wherein dielectric material fills spaces between the first portions of adjacent ones of the charge storage elements and includes a slot therein into which the control gates extend a distance between the first portions of adjacent charge storage elements.

30. (New) The non-volatile memory of claim 29, wherein the dielectric material between the first portions of adjacent ones of the charge storage elements is formed over the substrate surface.

31. (New) The non-volatile memory of claim 28, wherein the array includes memory cells that individually include, in a second direction across the array, two charge storage elements between adjacent substrate source and drain regions and a select transistor between the two charge storage elements, said second direction being perpendicular to said one direction.